

U.S. Patent Application No. 10/725,776
Attorney Docket No. 2102475-991290 (351991)

REMARKS

The Rejection under 35 U.S.C. § 103(a)

Claims 1, 3-4, 6, and 9-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,643,218 to *Chun*. Applicant respectfully traverses, noting that *Chun* does not disclose every element of Applicant's claims. More specifically, *Chun* does not disclose the generating of a precharge signal based on an active signal.

Chun discloses two semiconductor memory devices: prior art memory devices such as the ones shown in FIGS. 1-5, and a memory device according to its invention, shown in FIGS. 7 and beyond.

FIG. 1 illustrates the operation of memory devices that are prior art to *Chun*. Here, a conventional DRAM has a command decoder 26 that receives a write enable signal /WEI, and sends a corresponding write signal W to a precharge control signal generator 60. The precharge control signal generator 60 in turn generates a precharge control signal PRE for initiating the generation of a precharge. Thus, the prior art memory devices of *Chun* generate precharge signals based on a write enable signal /WEI. That is, the prior art of *Chun* discloses the generation of a precharge signal based on a write, or write enable, signal.

In the memory device of *Chun*, a synchronous memory device includes a CLK/CKE buffer 130 that receives externally-generated signals CLK and CKE, and generates a corresponding internal clock signal iCLK and internal clock enable signal iCKE (Col. 8:30-36). An asynchronous precharge control signal generator 140 then generates a precharge control signal PRE according to an internal precharge signal iPRE and the iCKE signal (Col. 8:54-60). Accordingly, "the precharge control signal PRE is generated by using the clock enable signal CKE . . ." (Col. 9:58-61). That is, the memory device of *Chun* discloses the generation of a precharge signal based on a clock enable signal.

As the various devices of *Chun* disclose the generation of a precharge signal based on either a write/write enable signal, or a clock enable signal, *Chun* does not disclose the generation of a precharge signal based on an active signal (See page 10, lines 2-4 of Applicant's specification for a description of an active signal). Indeed, Examiner notes that *Chun* does not disclose an active signal at all, necessarily implying that *Chun* also cannot disclose the

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generation of a precharge signal based on such an active signal. Accordingly, Applicant's claim 1 is patentable over *Chun* for at least the reason that it recites "generating an internal precharge signal to precharge the bit lines based on the active signal." Similarly, Applicant's claim 6 is patentable over *Chun* for at least the reason that it recites generating an internal precharge signal "in response to the active signal"

Claims 2-5 and 7-11 depend from claims 1 and 6 respectively, and are thus patentable over *Chun* for at least this same reason.

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CONCLUSION

In view of the above, it is respectfully submitted that Claims 1-11 are now in condition for allowance.

The Examiner is invited to call Applicant's attorney at the number below in order to speed the prosecution of this application.


The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to **Deposit Account No. 07-1896** and reference **Attorney Docket No. 2102475-991290 (351991)**.

Respectfully submitted,

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